

Amstrad "Joyce" software interface specification

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OCR'd by [Cliff Lawson](#), [Amstrad](#) - 8th June 97

(active low signals are shown as /<name>)

apologies for OCR errors esp. O=0 and n=h !!

Converted to HTML and minimally proofread for OCR errors by [Jacob Nevins](#), 10 June 1997. The original is available [here](#).

0 Related Documents

1. Zilog "Z80/Z80A CPU Technical Manual"
2. NEC "uPD765A Floppy Disc Controller Data Sheet"
3. AMSTRAD "Keyboard Controller Interface Spec."
4. AMSTRAD "Printer Controller Interface Spec."
5. AMSTRAD "Floppy Disc Drive Specs"
6. AMSTRAD "JOYCE Expansion Port Interface Spec."
7. INTERSIL IM6403 UART Data.

1 Introduction

This document defines the interface presented to the Z80 software by the Main Board hardware for the Amstrad "JOYCE" word processor.

The hardware design is based on the same architecture as the AMSTRAD "ANT" (Arnold Number Two) Colour personal computer, but uses a monochrome display, and no sound facilities other than a bleeper.

2 Summary

2.1 Processor

The processor is a Z80A-CPU running at a clock frequency of 4.00 MHz (+/-0.1%). There is logic that stretches /MREQ cycles using the processor /WAIT input during VDU accesses to the screen memory; this is the same as for the CPC464, but note that, unlike the CPC464, IORQ cycles are not stretched. The main board hardware does not make use of the processor's refresh counter, but expansion memory add-ons may use this feature.

2.1.1 Interrupts

The CPU may be interrupted on /NMI by requests from the floppy disc controller, and on /INT by requests from the floppy disc controller, the video timing controller and the external expansion bus.

Interrupts from the floppy disc controller to NMI and INT may be separately enabled and disabled under software control.

An interrupt for timing purposes is generated by the VDU controller during every vertical ('frame') flyback and every 52 scan lines thereafter until the next frame flyback, giving a timer period of 3.328 milliseconds for both 50Hz and 60Hz VDU systems. The interrupt is arranged to occur approximately 2 scans (128 microseconds) into the 26 scan (1664 microseconds) frame flyback status signal. When the software cannot respond immediately to these interrupts a readable hardware counter will record up to 15 missed interrupts. The counter is cleared automatically after reading.

2.2 Memory

2.2.1 Bootstrap Loading

There is no dedicated internal bootstrap ROM, but following a reset the printer controller is selected by hardware to supply the initial bootstrap program. This special bootstrap mode is terminated by an I/O command contained within the bootstrap program.

2.2.2 RAM

There are up to 2 megabytes of main memory, divided into 128 blocks of 16k each and designated blocks 0 to 127. In this document, blocks 0 to 7 are referred to as "standard" RAM, while blocks 8 to 127 are referred to as "expansion" RAM.

Any of the 128 memory blocks may be assigned to the four fixed 16k banks in CPU-addressable memory space 0000h to FFFFh, under software control; each 16k bank in CPU-addressable memory space may be configured for Read/Write access in any one memory block, except in the case of standard RAM where separate Read and Write access to different blocks is possible. Fast switching between separate Read and Write access and Read/Write access in standard RAM blocks may be accomplished by a one byte I/O command.

There may be either 128k, 256k or 512k bytes of dynamic RAM fitted internally, implemented as blocks 0 to 7, 0 to 15, or 0 to 31 respectively. Additional memory can be fitted externally on the expansion port up to a total system maximum of 2 megabytes.

The standard RAM is used in addition to the CPU for the monochrome VDU screen pixel memory, VDU scan line start address table, and the keyboard matrix keystate table.

2.2.3 VDU Screen Memory

The monochrome pixel display controller uses up to 22.5k bytes of the standard RAM as screen refresh memory. A 512 byte pointer table in the standard RAM, relocatable to start on any 512 byte boundary under software control of an I/O register, is used to hold the memory start addresses of the two hundred and fifty-six, 90 byte horizontal scan lines.

The display memory for one scan line consists of 90 bytes, starting at an address boundary for which A3 is 0. The VDU controller increments the memory address by eight between fetching bytes for display along the scan line; thus the pointer table may be arranged so that eight-scan characters occupy eight contiguous bytes in memory.

Each pair of bytes displayed contains sixteen, 1 bit pixels (P0 to P15) as follows:

A3	Bit	Pixel	A3	Bit	Pixel
==	===	=====	==	===	=====
0	D7	P0	1	D7	P8
0	D6	P1	1	D6	P9
0	D5	P2	1	D5	P10
0	D4	P3	1	D4	P11
0	D3	P4	1	D3	P12
0	D2	P5	1	D2	P13
0	D1	P6	1	D1	P14
0	D0	P7	1	D0	P15

On normal video display, a '0' pixel is displayed 'off' and a '1' pixel is displayed 'on'. When reverse video modes selected, the opposite is implied.

2.2.4 External Memory

Since the maximum total amount of main memory is 2 megabytes, up to 1,966,080 bytes of external expansion memory may be fitted on the expansion port of a 128k standard system, with correspondingly lower amounts for 256k and 512k systems. This external memory can be either RAM or EPROM. In addition for specialist and test purposes external EPROMs can be added that over-ride all other internal or external memory and the bootstrap system.

2.3 Input/Output Channel Summary

The standard interfaces on the processor board occupy I/O channels on the Z80 as follows:

ADDRESS	OUTPUT USE	INPUT USE
=====	=====	=====
00h	**Do Not Use**	Floppy Disc Status
01h	Floppy Disc Data	Floppy Disc Data
02h-7Fh	**Do Not Use**	**Do Not Use**
80h-EFh	Expansion Port	Expansion Port
F0h	0000h-3FFFh Mem. Map	**Do Not Use**
F1h	4000h-7FFFh Mem. Map	**Do Not Use**
F2h	8000h-BFFFh Mem. Map	**Do Not Use**
F3h	C000h-FFFFh Mem. Map	**Do Not Use**
F4h	Mem. Map R/W Control	Timer Interrupt Counter
F5h	VDU Pointer Table Addr.	**Do Not Use**
F6h	VDU Pointer Top Scan	**Do Not Use**
F7h	VDU Video Control	**Do Not Use**
F8h	System Control	System Status
F9h	**Do Not Use**	UART Status (Prototype)
FAh	**No Effect**	**Undefined**
FBh	**No Effect**	**Undefined**
FCh	Printer Data	Printer Data
FDh	Printer Commands	Printer Status
FEh	UART Data (Prototype)	UART Data (Prototype)

Command 0 will terminate the bootstrap mode in which all "memory" fetch cycles are from the printer controller data port instead of the memory. No data should be sent to the printer controller during bootstrap mode.

Command 1 will cause the hardware to generate an immediate system reset and pulse the reset line on the expansion bus.

Command 2 will enable non-maskable interrupts from the Floppy Disc Controller until Command 3 is issued to enable maskable interrupts instead, or Command 4 is issued to disable all interrupts from the Floppy Disc Controller, or until the first non-maskable interrupt occurs. On power-up and system reset all Floppy Disc Controller Interrupts are disabled.

Command 5 will set the Floppy Disc Controller Terminal Count input true (high) until Command 6 is issued to clear it. On power-up and system reset Terminal Count is set true.

Command 8 will float the video output signal allowing video information to be supplied externally via the expansion port, until Command 7 is issued to return to internally driven video. On power-up and system reset video will be driven internally.

Command 9 will switch the disc drive motor(s) on until Command 10 is issued to switch the motor(s) off. On power-up and system reset the disc motor(s) will be switched off.

Command 11 will switch on the built-in bleeper until Command 12 is issued to switch it off. On power-up and system reset the bleeper is switched off.

4 Timer Interrupt Counter Input Channel

This channel may be read to 'catch up' in situations where interrupts from the timer must not be missed, but cannot be processed immediately because the operation in hand is too important to be interrupted by the timer.

Bit ===	Input Use =====
D7	Undefined
D6	Undefined
D5	Undefined
D4	Undefined
D3	Timer Interrupt Counter C3
D2	Timer Interrupt Counter C2
D1	Timer Interrupt Counter C1
D0	Timer Interrupt Counter C0

The timer interrupt count C3-C0 indicates the number of timer interrupts that should have occurred since the counter was last read; any bit set in the counter causes an interrupt to the CPU, and the counter will never increment beyond a count of fifteen. (NOTE! The counter is synchronized by two CPU instruction fetch cycles (M1). If the M1 of a counter read command latches a new pending timer interrupt, the counter will not at the time of the read operation have been incremented, and therefore this new interrupt will be lost). On power-up and system reset the counter is cleared.

5 Printer Controller

This controls the built-in matrix printer as well as providing the bootstrap program for the Z80 CPU. During bootstrap mode, when all transfers are data (rather than status or command), no data should be sent to the printer controller.

For further information see the specific printer controller documentation (unavailable!).

6 765 Floppy Disc Controller

The floppy disc controller supports one or two 3 inch single- or double-sided double-density floppy disc drives with a data rate of 250 kilobits per second.

The hardware system imposes the following restraints on the use of the 765 controller and disc drives:

1. The clock frequency of the 765 is fixed at 4.0 MHz.
2. There is no DMA implemented, but the 765's INT output may be used to drive the /INT and /NMI inputs of the Z80 CPU.
3. Drive 0 is always present. Drive 1 is optional. Drives 2 and 3 are not implemented and should never be accessed. When Drive 1 is accessed but not fitted, Drive Ready and Write Protected status signals from Drive 1 are false. When Drive 1 fitted and accessed with no disk inserted, Drive Ready status from Drive 1 is false and Write Protected status from Drive 1 is true.
4. The FAULT signal from the disc drive(s) to the 765 is forced permanently false.
5. The Two-Sided status signal from the drive(s) is not provided, but the interface to the drives allows the use of double-sided drives.
6. No write precompensation is provided.

Control and sensing of disc controller interrupts, disc drive motor control, and terminal count may be achieved by the use of the System Control and Status I/O channel.

7 VDU Controller

The VDU Controller provides a monochrome pixel display. At 50 Hz frame rate, 256 scan lines are displayed, and at 60 Hz frame rate, 200 scan lines are displayed. A system of indirection pointers for scan line control allows rapid rolling and scrolling of the display.

7.1 VDU Video Control Register

This write-only register is organised as follows:

Bit	Output Use
===	=====
D7	Display Reverse Video
D6	Enable Video
D5	No Effect
D4	No Effect
D3	No Effect
D2	No Effect

D1	No Effect
D0	No Effect

Writing a 1 to bit D7 will switch the screen display into reverse video, (in which each '1' pixel is displayed 'off', each '0' pixel is displayed 'on', and the surrounding border is displayed 'on'), until a 0 is written to switch the screen display back to normal video. On power-up and system reset normal video will be selected.

Writing a 1 to bit D6 will enable the video until a 0 is written to disable the video (when the screen will be blanked). On power-up and system reset the video will be disabled. Note that a 'blank' reverse video display implies that all pixels and surrounding border are forced 'on'.

7.2 Scan Line Pointer Table

Two write-only registers are used to specify the address of the scan line pointer table and the 2 byte entry to be used for the top scan line of the pixel display.

7.2.1 Pointer Table Address Register

Bit	Output Use
===	=====
D7	B2
D6	B1
D5	B0
D4	A13
D3	A12
D2	A11
D1	A10
D0	A9

B2 to B0 specify the number of the standard 16k memory block in which the pointer table is to reside.

A13 to A9 specify which 512 byte section of the block is to be used. The pointer table occupies the whole 512 byte section.

To avoid unsightly effects on the screen this register should only be updated during frame flyback time.

7.2.2 Pointer Table Top Scan Register

Bit	Output Use
===	=====
D7	A8
D6	A7
D5	A6
D4	A5
DB	A4
D2	A3
D1	A2
D0	A1

A8 to A1 specify which 2 byte entry in the pointer table is to be used for the top scan line. Entries for subsequent scan lines follow in order, wrapping around at the end of the 512 byte section of memory if the first entry is not for the first scan line.

To avoid unsightly effects on the screen this register should only be updated during frame flyback time.

7.2.3 Pointer Table Format

The pointer table consists of 256 entries each of 2 bytes interpreted by the VDU controller as follows:

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	LP8	LP7	LP6	LP5	LP4	LP2	LP1	LP0
1	LB2	LB1	LB0	LP13	LP12	LP11	LP10	LP9

These two bytes define the position in standard RAM of the 90 bytes of pixel information to be used for this scan line. LB2 to LB0 specify the number of the standard 16k block containing this information. LP3 is always zero. LP13 to LP0 specify the starting address within the block such that the first byte of pixel information is at an address that is LP0-LP13 in bytes from the beginning of the block. Thus the line can start on any byte boundary with A3 = 0 within the block.

To avoid unsightly effects on the screen the table should only be updated during frame flyback time.

8 Memory Map Control

8.1 Memory Mapping Registers

There are four memory mapping registers, one for each 16k bank of CPU-addressable memory space. Each register is used to define which of the eight standard 16k memory blocks is to be used for read access and also which is to be used for write access, or alternatively which of 120 possible expansion memory blocks is to be used for read/write access:

Bit	Output	Use
===	=====	
D7	/Standard Block	or Expansion Block
D6	RB2	EX6
D5	RB1	EX5
D4	RB0	EX4
D3	Ignored	EX3
D2	WB2	EX2
D1	WB1	EX1
D0	WB0	EX0

Bits D6-D0 select standard memory blocks when a 0 is written to D7 and an expansion memory block when a 1 is written to D7. RB2-RB0 is the standard block to be used for read access. WB2-WB0 is the standard block to be used for write access. EX6-EX0 is the expansion block to be used for read/write access.

Expansion blocks 8 to 31, if present, may be fitted either internally, or externally on the expansion port, whereas expansion blocks 32 to 127, if present, are always fitted externally. The total amount of memory in a system always consists of a number of contiguous memory blocks.

If an absent expansion block is selected, an internal block will be accessed in its place for both read and write; which block this is depends on the amount of internal memory fitted as follows:

Internal Memory Size =====	Substituted Block Number =====
128 k (Standard)	EX2-EX0
256 k	EX3-EX0
512 k	EX4-EX0

If an expansion block is selected in the range 0 to 7, the corresponding standard block will be accessed for both read and write.

The contents of the memory mapping registers are undefined on power-up.

8.2 Memory Mapping Read/Write Control Register

In addition to the memory mapping registers there is a read/write control register which allows software to force the same standard block to be used for read and write access without changing the memory mapping register contents. This register is structured as follows:

Bit ===	Output use =====
D7	RW3 (CPU bank C000h to FFFFh)
D6	RW0 (CPU bank 0000h to 3FFFh)
D5	RW2 (CPU hank B000h to BFFFh)
D4	RW1 (CPU bank 4000h to 7FFFh)
D3	No effect
D2	No effect
D1	No effect
D0	No effect

If the RW bit for a particular memory address area is set to a 1 then both read and write access occurs to the standard block specified by the relevant WB2-WB0 block number, the RB2-RB0 block number being ignored. The contents of this register are undefined on power-up.

[\[note 1\]](#)

9 Keyboard Interface

Data from the keyboard is written automatically into a table occupying the top sixteen bytes of block 3 of the standard RAM. Further information on the format of these bytes can be found in the keyboard controller documentation.

10 IM6403 UART (on prototype systems only)

This device operates at 9600 baud with 8 bit serial data input and output with no parity and one stop bit. Refer to the manufacturer's data for operation and explanation of status bits.

The status input channel is organised as follows:

Bit ===	Input Use =====
D7	DR
D6	PE
D5	FE
D4	OE
D3	Always 0 on prototype system.
D2	Not Switch SW1 Pressed
D1	TRE
D0	TBRE

[\[note 2\]](#)

After this document was released Richard Clayton of Locomotive posted some [comments](#).

Note 1 on section 8.2:

Those people writing emulators may wish to ignore section 8.2. These features were never used (intentionally anyway) by any Locomotive software, and were never made public so I seriously doubt that any third party software used this.

Experts on the CPC464 architecture will understand why they are there, and will be interested to know that they were present for the ANT to use (and that part of the gate array was identical between the two machines). I believe that memory expansion boards (to which this is relevant) will not honour these commands - so I would not recommend anyone to write software to use these features now.

Note 2 on section 10:

I think I may still have a board somewhere in an attic to which section 10 is relevant... others should ignore it completely!