(c) K. Mueller 2024
CPU MMU Clk PCB
Rev. 1.1.1
DESIGNED WITH
KiCad Ver. 7.0
Pin-Header horizontal - PCW-Systembus P1
49
50
1
2
U1 74HCT02
Z80CPU
U6
C2 100nF
100nF C13
C7 100nF
C8 100nF
R2 4k7
U3
EPM7128S
C5 100nF
C3
Jumper set = '0'
CF-PORT J4
MMU-PORT J5
R1 10k
RN1 8x10k0
J3 JTAG
C11 100nF
RN3 8x10k0 100nF
SRAM-Expansion-Conn.
J7
U4 74LS245
C10
C1 100nF
J1